Notice of Allowability	Application No.	Applicant(s)	
	10/064,582	GOODNOW ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 10/03/2005 and amendment filed on 07/11/2005*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☑ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Steven Fischman on 3/20/2006.

The application has been amended as follows:

In claim 11, to correct a lack of antecedent basis for "said transmitter means", in line 4 of claim 11, after "successively transmitting data signals", "by a transmitter means" is inserted.

Allowable Subject Matter

2. Claims 1-18 are allowed.

3. Applicants' RCE (Request for Continued Examination) filed on 10/03/2005 and the amendment filed on 07/11/2005 have been entered.

4. The drawings filed on 07/11/2005 have been accepted.

5. The following is an examiner's statement of reasons for allowance:

The present invention pertains generally to timing systems for integrated circuits and more specifically, to novel circuits for altering the clock speed used to send and receive data within the IC based on physical characteristics of the IC.

The claimed invention (claim 1 as representative) recites features such as:"...providing a clock timing signal to respective said transmitter means and said receiver device, said clock timing signal used for timing said data signal transmission and reception within said IC at successively different clock speeds, each said successive data signal transmission transmitted at a different clock speed; a monitoring circuit means for receiving successive data signal transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed; and, means for adjusting said clock timing signal provided to respective said transmitter means and said receiver device at each clock speed, said means adjusting said clock timing signal to achieve a maximum speed allowed for the IC that avoids said data transmission fail point during real-time operation."

The prior art of record (Tamura et al. US 6,247,138 B1) teach a timing signal generating circuit (col. 4, line 66, Tamura et al.). Tamura et al. also teach that as shown in FIG. 11, in the signal transmission system according to the second aspect of the present invention, signals are transmitted using the plurality of signal lines (data signal lines) 521 to 52n; that is, the data (signals) DD1 to DDn are supplied to the timing adjusting circuits (timing adjusting means) 531 to 53n at the receiving end via the respective transmitting drivers 511 to 51n and data signal lines 521 to 52n (fig. 11, col. 18, lines 9-16, Tamura et al.). Tamura et al. teach that the timing adjusting circuits 531 to 53n optimize the signal latch timing at the respective input latches 541 to 54n according to the skew on each of the signal lines 521 to 52n, as shown in FIG. 13. More specifically, the strobe signal (clock) clk1 whose timing is adjusted by the timing adjusting circuit 531 by considering the skew due to the signal line 521, etc. is supplied to the input latch 541 that latches the data DD1; the strobe signal clk2 whose timing is adjusted by the timing adjusting circuit 532 by considering the skew due to the signal line 522 etc. is supplied to the input latch 542 that latches the data DD2; and the strobe signal clkn whose timing is adjusted by the timing adjusting circuit 53n by considering the skew due to the signal line 52n, etc. is supplied to the input latch 54n that latches the data DDn (fig. 11, 13, col. 18, lines 37-52, Tamura et al.).

Sasaki et al. (US 2002/0114224 A1) teach a design method and a design system of semiconductor integrated circuits. Sasaki et al. teach performing adjustment of clock timing for each flip-flop in the semiconductor integrated circuit such that flip-flop to flip-flop data transmission can be performed in a target machine cycle (page 2, paragraphs 14-15, Sasaki et al.).

Naffziger et al. (US 6,509,788 B2) teach that the present invention is directed to a system and method, which utilize an on-chip oscillator to provide the appropriate clock frequency for components of the chip to manage power consumption by the chip. An on-chip oscillator is utilized to provide the clock frequency for the chip's core circuitry, and such oscillator can dynamically adjust such clock frequency to manage the chip's power consumption (col. 4, lines 9-16, Naffziger et al.).

Fukazawa (US 6,655,588 B2) teaches that there is provided a card system wherein when data is transmitted and received over a signal line between and IC card and a card reader/writer for reading or writing of the data, a data transmitting side transmits a parity based upon content of the data together with

the data over the signal line and a data receiving side checks whether or not there is any error in reception of data based upon content of the data and the parity received to transmit back to the data transmitting side a data retransmission request signal for requesting the data transmitting side to retransmit the data when there is an error (col. 5, lines 33-43, Fukazawa).

However the prior arts of record do not teach providing a clock timing signal to respective said transmitter means and said receiver device, said clock timing signal used for timing said data signal transmission and reception within said IC at successively different clock speeds, each said successive data signal transmission transmitted at a different clock speed; a monitoring circuit means for receiving successive data signal transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed; and, means for adjusting said clock timing signal provided to respective said transmitter means and said receiver device at each clock speed, said means adjusting said clock timing signal to achieve a maximum speed allowed for the IC that avoids said data transmission fail point during real-time operation.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 1 is allowable over the prior arts of record. Claims 2-10 are allowed because of the combination of additional limitations and the limitations listed above.

- Claim 11 recites similar features as in claim 1. Thus claim 11 is allowable over the prior arts of record. Claims 12-18 are allowed because of the combination of additional limitations and the limitations listed above.
- Thus, claims 1-18 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

GUY LAMARRE
PRIMARY EXAMINER